REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Boilerplate update, added appendix B for die. ksr	01-05-01	Raymond Monnin
B	Boilerplate update and part of five year review. tcr	06-01-19	Raymond Monnin
C	Changes made to paragraph 1.4, added 3.2.7.1, and added test to Table IA. ksr	06-10-02	Raymond Monnin
D	Updated drawing to meet current MIL-PRF-38535 requirements. Removed class M references Updated Figure 4 to reflect vendor's current modeling and testing methods. Corrected Case Y figure and dimensions. - glg	14-02-11	Charles Saffle
E	Add supply voltage ramp time to section 1.4. Updated table IB to reflect vendor's current modeling and testing methods. - glg	14-05-01	Charles Saffle
F	Corrections to paragraph 1.6. Addition of paragraph 4.4.4.5. - glg	14-06-24	Charles Saffle
G	Update to reflect current MIL-PRF-38535 requirements. Corrected 1.6, Figure 1, and 6.7. – llb	19-05-28	Charles Saffle

REV																				
SHEET																				
REV	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30				

REV STATUS	REV	G	G	G	G	G	G	G	G	G	G	G	G	G
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Gary L. Gross

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Jeff Bowling

APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
99-03-02

REVISION LEVEL
G

MICROCIRCUIT, MEMORY, DIGITAL, RADIATION-HARDENED, CMOS/SOI, 128K X 8 STATIC RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-98537**

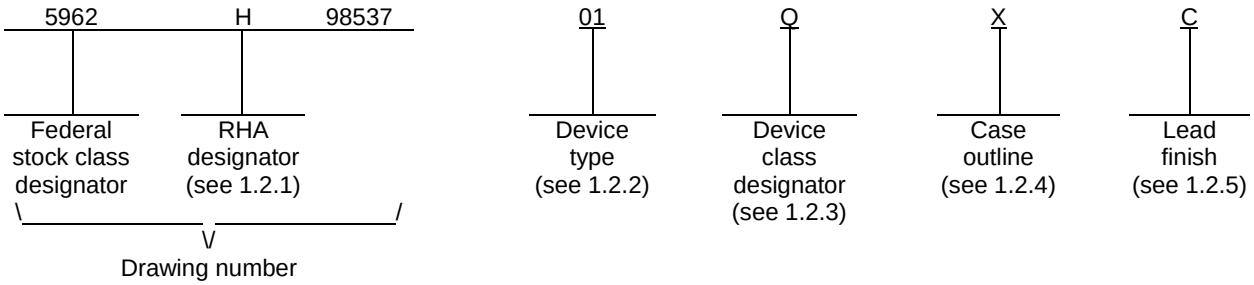
SHEET 1 OF 30

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Input/output levels	Chip enable	Access time
01		128K X 8 Rad-Hard CMOS/SOI SRAM	CMOS	Dual	25 ns
02		128K X 8 Rad-Hard CMOS/SOI SRAM	TTL	Dual	25 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	32	Flat pack
Y	See figure 1	40	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Generic numbers are listed on the Standard Microcircuit Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-HDBK-103.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +6.5 V dc
DC input voltage range (V_{IN})	-0.5 V dc to VCC + 0.5 V dc 4/
DC output voltage range (V_{OUT})	-0.5 V dc to VCC + 0.5 V dc 4/
Storage temperature range	-65°C to +150°C
Case operating temperature range	-55°C to +125°C
Lead temperature (soldering 5 seconds)	+270°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case X and Y	2.0°C/W
Output voltage applied to High-Z state	-0.5 V dc to V_{CC} + 0.5 V dc
Maximum power dissipation	2.0 W
Maximum junction temperature	+175°C

1.4 Recommended operating conditions. 4/

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Supply voltage reference (GND)	0.0 V
Supply voltage ramp time (0 V to V_{CC})	50 ms
High level input voltage range (V_{IH}):	
Device type 01 (CMOS levels)	0.7 x V_{CC} to V_{CC} + 0.3 V dc
Device type 02 (TTL levels)	2.2 V dc to V_{CC} + 0.3 V dc
Low level input voltage range (V_{IL}):	
Device type 01 (CMOS levels)	-0.3 V dc to 0.3 x V_{CC}
Device type 02 (TTL levels)	-0.3 V dc to 0.8 V dc
Case operating temperature range	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, method 5012)	100 percent

1.6 Radiation features.

Maximum total dose available (dose rate = 50-300 rad/s)	1 Mrads(Si)
Single event phenomenon (SEP) (see 4.4.4.4):	
Heavy ion test:	
No SEL occurs at effective LET	≤ 120 MeV-cm^2/mg
SEU error rate	1.0 x 10^{-10} upsets/bit-day 5/
Neutron irradiation	1.0 x 10^{14} neutrons/cm^2 6/

2/ Stresses above the absolute maximum rating may cause permanent damage to the device.
3/ All voltage are referenced to GND.
4/ Maximum applied voltage shall not exceed +6.5 V.
5 Based on CREME96 results for a geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield. Weibull parameters are available from the vendor to calculate projected upset rates for other orbits/environments (such as Adams 90% worst case) and using different upset rate calculating programs (such as Space Radiation 5.0).
6/ Guaranteed, but not tested.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see Appendix B to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Output load circuit. The output load circuit shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 Radiation exposure circuit. The radiation test circuit shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request.

3.2.7 Functional tests. Various functional tests used to test this device are contained in the appendix A herein. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.2.7.1 Supply voltage ramp rate and functionality. The part utilizes column and row sparing (redundancy). Slow V_{CC} ramp rates may fail to activate necessary sparing. The device is tested with a Read/Write March pattern after power-up at 50 ms and 2 seconds to insure proper operation.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -5 mA, V_{IL} = 1.35 V, V_{IH} = 3.15 V	1, 2, 3	01	4.2		V
		M, D, P, L, R, F, G, H	1 1/		2/		
		V_{CC} = 4.5 V, I_{OH} = -4 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	02	4.2		
		M, D, P, L, R, F, G, H	1 1/		2/		
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 10 mA, V_{IL} = 1.35 V, V_{IH} = 3.15 V	1, 2, 3	01		0.4	V
		M, D, P, L, R, F, G, H	1 1/			2/	
		V_{CC} = 4.5 V, I_{OL} = 8 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	02		0.4	
		M, D, P, L, R, F, G, H	1 1/			2/	
Input leakage current	I_{ILK}	0 V ≤ V_{IN} ≤ 5.5 V, V_{CC} = 5.5 V	1, 2, 3	All	-5	5	µA
		all other pins at 0.0 V M, D, P, L, R, F, G, H	1 1/		2/	2/	
Output leakage current	I_{OLK}	0 V ≤ V_{OUT} ≤ 5.5 V, V_{CC} = 5.5 V	1, 2, 3	All	-10	10	µA
		all other pins at 0.0 V M, D, P, L, R, F, G, H	1 1/		2/	2/	
Operating supply current	I_{DDOPW}	f = 40 MHz, NWE = GND, CE, NOE = V_{CC}	1, 2, 3	All		240	mA
		M, D, P, L, R, F, G, H	1 1/			2/	
Supply current (deselected)	I_{DDSB}	f = 0 MHz, NCS, CE, NOE, NWE = V_{CC}	1, 2, 3	All		2.0	mA
		M, D, P, L, R, F, G, H	1 1/			2/	
Supply current (standby)	I_{DDSBMF}	f = f_{MAX} 3/, CE = GND, NCS, NOE, NWE = V_{CC}	1, 2, 3	All		2.0	mA
		M, D, P, L, R, F, G, H	1 1/			2/	
Data retention current	I_{DR}	V_{CC} = 2.5 V	1, 2, 3	All		700	µA
		M, D, P, L, R, F, G, H	1 1/			2/	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Input capacitance 2/ 4/	C_{IN}	V_{IN} = 0.0 V or 5.5 V, f = 1.0 MHz, T_A = 25°C, see 4.4.1e	4	All		7	pF
Output capacitance 2/ 4/	C_{OUT}	V_{OUT} = 0.0 V or 5.5 V, f = 1.0 MHz, T_A = 25°C, see 4.4.1e	4	All		9	pF
Functional tests		See 4.4.1c	7, 8A, 8B	All			
		M, D, P, L, R, F, G, H	7 1/		2/	2/	
Supply voltage ramp time	Ramp50ms Ramp2s	Ramp from 0 V to V_{CC} in 50 ms Ramp from 0 V to V_{CC} in 2 s	7, 8A, 8B	All			
		M, D, P, L, R, F, G, H	7 1/		2/	2/	
Data retention voltage	V_{DR}	V_{CC} = 2.5 V	7, 8A, 8B	All	5/		V
		M, D, P, L, R, F, G, H	1 1/		2/		
Read cycle time	t_{AVAV}	See figures 4 and 5	9, 10, 11	All	25		ns
		M, D, P, L, R, F, G, H	9 1/		2/		
Address access time	t_{AVQV}		9, 10, 11	All		25	ns
		M, D, P, L, R, F, G, H	9 1/			2/	
Chip select access time	t_{SLQV}		9, 10, 11	All		25	ns
		M, D, P, L, R, F, G, H	9 1/			2/	
Chip enable access time	t_{EHQV}		9, 10, 11	All		25	ns
		M, D, P, L, R, F, G, H	9 1/			2/	
Output enable access time	t_{GLQV}		9, 10, 11	All		9	ns
		M, D, P, L, R, F, G, H	9 1/			2/	
Output enable to output disable	t_{GHQZ}		9, 10, 11	All		9	ns
		M, D, P, L, R, F, G, H	9 1/			2/	
Chip select to output active	t_{SLQX}		9, 10, 11	All	5		ns
		M, D, P, L, R, F, G, H	9 1/		2/		
Chip enable to output active	t_{EHQX}		9, 10, 11	All	5		ns
		M, D, P, L, R, F, G, H	9 1/		2/		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Output enable to output active	t_{GLQX}	See figures 4 and 5	9, 10, 11	All	0		ns
		M, D, P, L, R, F, G, H	9 1/		2/		
Output hold after address change	t_{AXQX}		9, 10, 11	All	3		ns
		M, D, P, L, R, F, G, H	9 1/		2/		
Chip select to output disable	t_{SHQZ}		9, 10, 11	All		10	ns
		M, D, P, L, R, F, G, H	9 1/			2/	
Chip disable to output disable	t_{ELQZ}		9, 10, 11	All		10	ns
		M, D, P, L, R, F, G, H	9 1/			2/	
Write cycle time 6/	t_{AVAV}		9, 10, 11	All	25		ns
		M, D, P, L, R, F, G, H	9 1/		2/		
Address setup to end of write	t_{AVWH}		9, 10, 11	All	20		ns
		M, D, P, L, R, F, G, H	9 1/		2/		
Chip select to end of write	t_{SLWH}		9, 10, 11	All	20		ns
		M, D, P, L, R, F, G, H	9 1/		2/		
Chip enable to end of write	t_{EHWH}		9, 10, 11	All	20		ns
		M, D, P, L, R, F, G, H	9 1/		2/		
Write pulse width access time	t_{WLWH}		9, 10, 11	All	20		ns
		M, D, P, L, R, F, G, H	9 1/		2/		
Data setup to end of write	t_{DVWH}		9, 10, 11	All	15		ns
		M, D, P, L, R, F, G, H	9 1/		2/		
Data hold after end of write	t_{WHDX}		9, 10, 11	All	0		ns
		M, D, P, L, R, F, G, H	9 1/		2/		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Address setup to start of write	t_{AVWL}	See figures 4 and 5 6/ 7/	9, 10, 11	All	0		ns
		M, D, P, L, R, F, G, H	9 1/		2/		
Address hold after end of write	t_{WHAX}		9, 10, 11	All	0		ns
		M, D, P, L, R, F, G, H	9 1/		2/		
Output active after end of write	t_{WHQX}		9, 10, 11	All	5		ns
		M, D, P, L, R, F, G, H	9 1/		2/		
Write enable to output disable	t_{WLQZ}		9, 10, 11	All		9	ns
		M, D, P, L, R, F, G, H	9 1/			2/	
Write disable pulse width	t_{WHWL}		9, 10, 11	All	5		ns
		M, D, P, L, R, F, G, H	9 1/		2/		

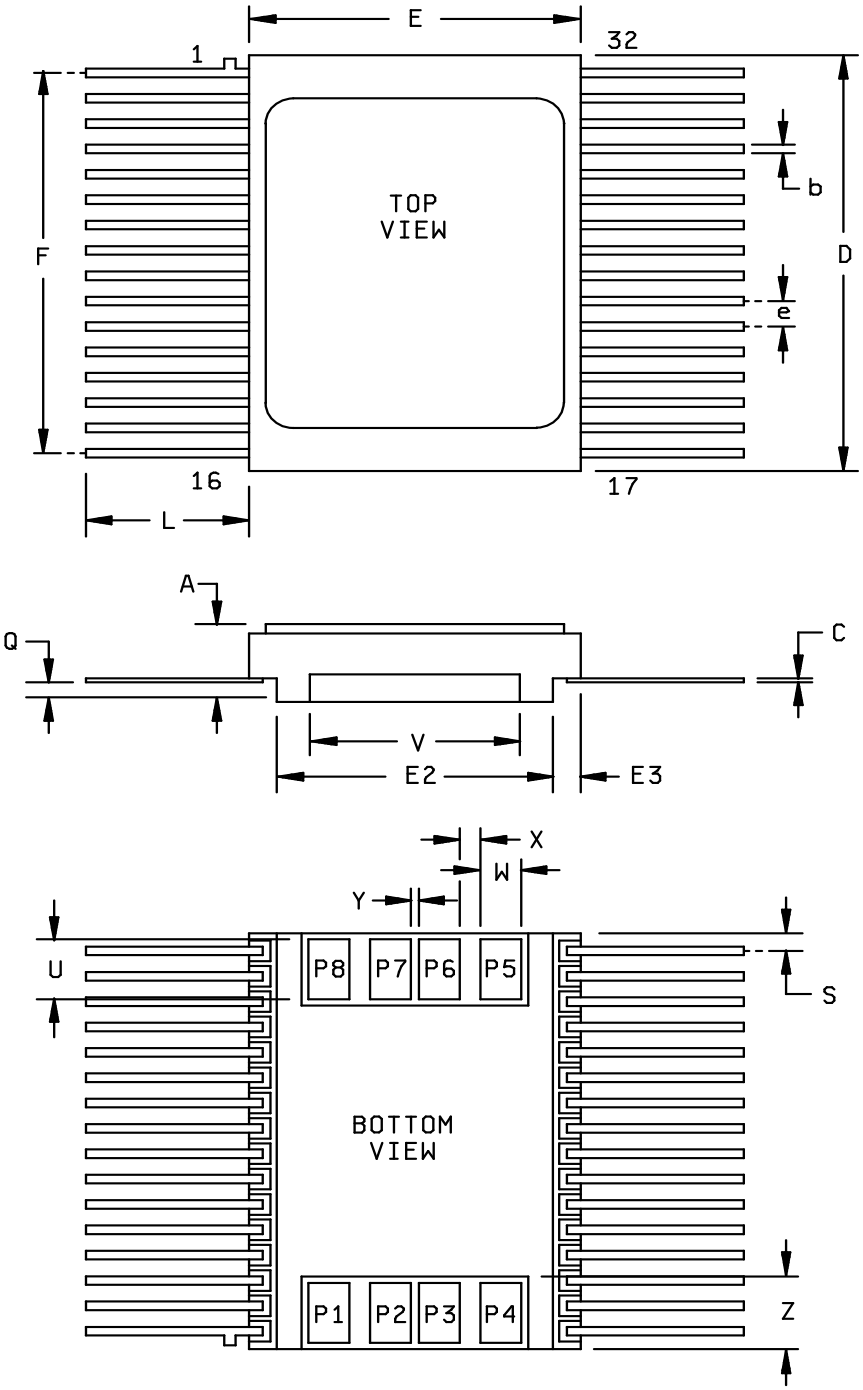
1/ When performing postirradiation electrical measurements for any RHA level $T_A = +25°C$. Limits shown are guaranteed at $T_A = +25°C \pm 5°C$. The M, D, P, L, R, F, G, and H in the test condition column are the postirradiation limits for the device types specified in the device types column.
2/ Preirradiation values for RHA marked devices shall also be the postirradiation values unless otherwise specified.
3/ $f_{MAX} = 1/t_{AVAV}(min)$.
4/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in table IA.
5/ As verified by functional test.
6/ $t_{AVAV} = t_{WLWH} + t_{WHWL}$

TABLE IB. SEP test limits. 1/ 2/

Device type	Ion type	Memory pattern	$V_{CC} = 4.5\ V$ SEU error rate Adam's 90% worst-case environment 3/	Bias for latch-up test $V_{CC} = 5.5\ V$, no SEL at effective LET = 4/
All	Heavy Ion	5/	1.0×10^{-10} upsets/bit-day	LET ≤ 120 MeV-cm^2/mg

1/ For SEP test conditions, see 4.4.4.3 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Based on CREME96 results for a geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield. Weibull parameters are available from the vendor to calculate projected upset rates for other orbits/environments (such as Adams 90% worst case) and using different upset rate calculating programs (such as Space Radiation 5.0).
4/ Worst case temperature $T_A = +125°C \pm 10°C$ for latch up.
5/ Testing shall be performed using checkerboard and checkerboard bar test patterns.

Case X



NOTE: Parts are delivered with leads unformed. Lid is tied to GND.

FIGURE 1. Case outlines.

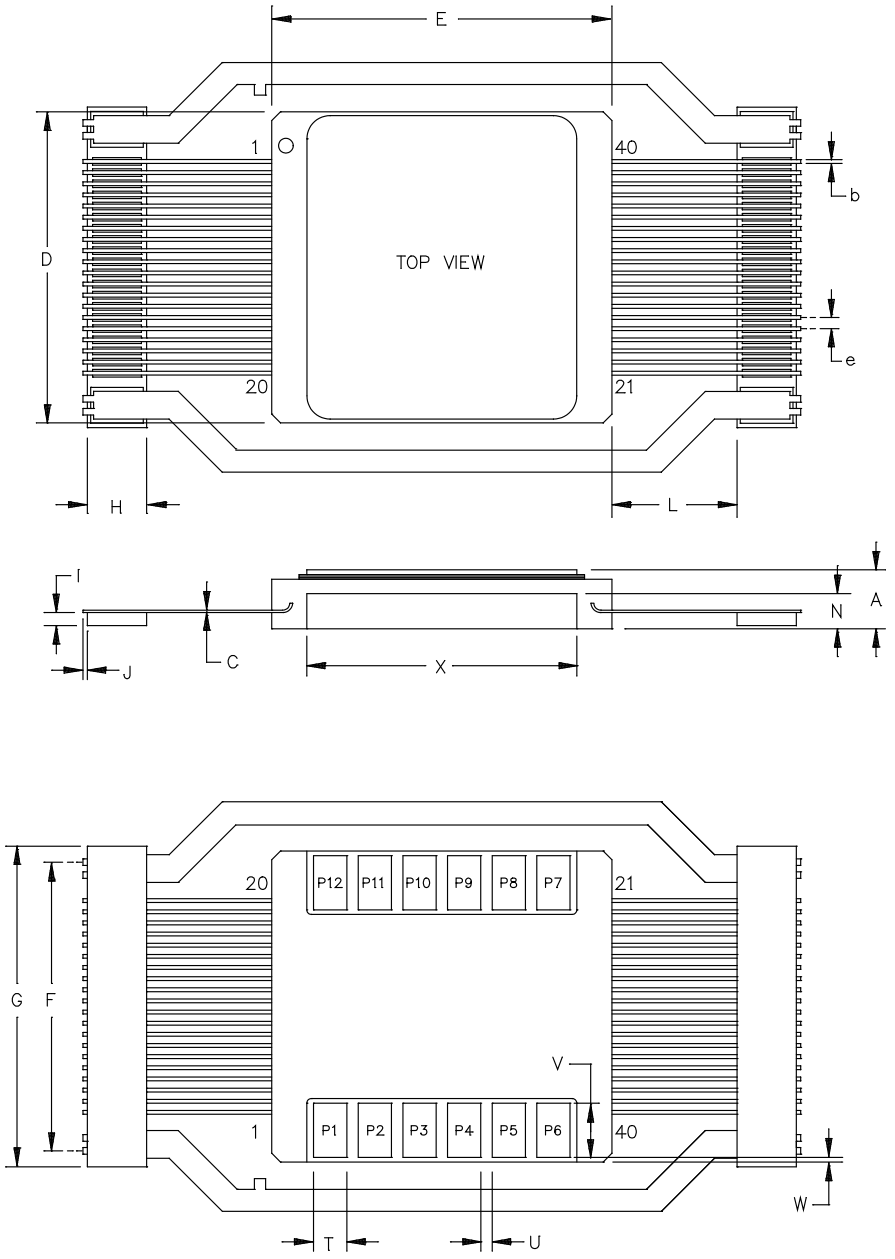
Case X

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.048	3.810	0.120	0.150
b	0.381	0.483	0.015	0.019
C	0.102 to 0.223		0.004 to 0.009	
D	20.625	21.031	0.812	0.828
e	1.143	1.397	0.045	0.055
E	15.037	15.443	0.592	0.608
E2	12.497	12.903	0.492	0.508
E3	1.016 ref.		0.040 ref.	
F	18.923	19.177	0.745	0.755
L	7.493 min.		0.295 min.	
Q	0.660 to 1.143		0.026 to 0.045	
S	0.635	1.143	0.025	0.045
U	2.032 ref.		0.080 ref.	
V	9.652 ref.		0.380 ref.	
W	1.27 ref.		0.050 ref.	
X	1.905 ref.		0.075 ref.	
Y	0.254 ref.		0.010 ref.	
Z	3.429 ref.		0.135 ref.	

NOTE: Although dimensions are in inches, the US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the two, the inch-pound units shall take precedence. Metric equivalents are for general information only.

FIGURE 1. Case outline - Continued.

Case Y



NOTE: Parts are delivered with leads unformed. Lid is tied to GND.

FIGURE 1. Case outlines – Continued.

Case Y

Symbol	Millimeters			Inches		
	Min	Nom.	Max	Min	Nom.	Max
A	2.95	3.30	3.66	0.116	0.130	0.144
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.114	0.15	0.191	.0045	0.006	0.0075
D	17.78	18.03	18.29	0.700	0.710	0.720
E	19.51	19.69	19.860	0.768	0.775	0.782
e	0.580	.64	0.690	0.023	0.025	0.027
F	11.94	12.07	12.19	0.470	0.475	0.480
G	19.10	19.30	19.51	0.752	0.760	0.768
H	3.30	3.43	3.56	0.130	0.135	0.140
I	0.64	0.76	0.89	0.025	0.030	.035
J			.254			0.010
L	6.83	7.24	7.62	.270	0.285	0.300
N	1.17	1.27	1.37	.046	0.050	0.054
T		1.63			0.064	
U		0.15			0.006	
V		3.18			0.125	
W		.127			0.005	
X		12.7			0.500	

NOTE: Although dimensions are in inches, the US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the two, the inch-pound units shall take precedence. Metric equivalents are for general information only.

FIGURE 1. Case outline – Continued.

Device type	All	
Case outline	X	Y
Terminal number	Terminal symbol	
1	NC	A16
2	A16	GND
3	A14	V_{CC}
4	A12	A14
5	A7	A12
6	A6	A7
7	A5	A6
8	A4	A5
9	A3	A4
10	A2	A3
11	A1	A2
12	A0	A1
13	DQ0	A0
14	DQ1	DQ0
15	DQ2	DQ1
16	GND	DQ2
17	DQ3	NC
18	DQ4	V_{CC}
19	DQ5	GND
20	DQ6	NC
21	DQ7	NC
22	NCS	GND
23	A10	V_{CC}
24	NOE	DQ3
25	A11	DQ4
26	A9	DQ5
27	A8	DQ6
28	A13	DQ7
29	NWE	NCS
30	CE	A10
31	A15	NOE
32	V_{CC}	A11
33	---	A9
34	---	A8
35	---	A13
36	---	CE
37	---	NWE
38	---	V_{CC}
39	---	GND
40	---	A15
P1	V_{CC}	V_{CC}
P2	GND	GND
P3	GND	GND
P4	V_{CC}	V_{CC}
P5	V_{CC}	V_{CC}
P6	GND	GND
P7	GND	GND
P8	V_{CC}	V_{CC}
P9		V_{CC}
P10		GND
P11		GND
P12		V_{CC}

Note: P1 through P12 refer to pads on devices, see Figure 1 case outlines.

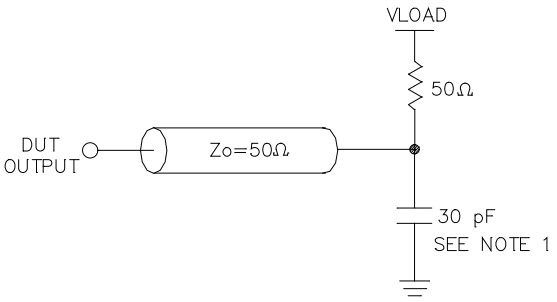
FIGURE 2. Terminal connections.

Mode	Inputs 1/ 2/					Power
	CE	NCS	NWE	NOE	I/O	
Write	High	Low	Low	X	Data in	Active
Read	High	Low	High	Low	Data out	Active
Standby	X	High	X	X	High Z	Standby
Standby 3/	Low	X	X	X	High Z	Standby

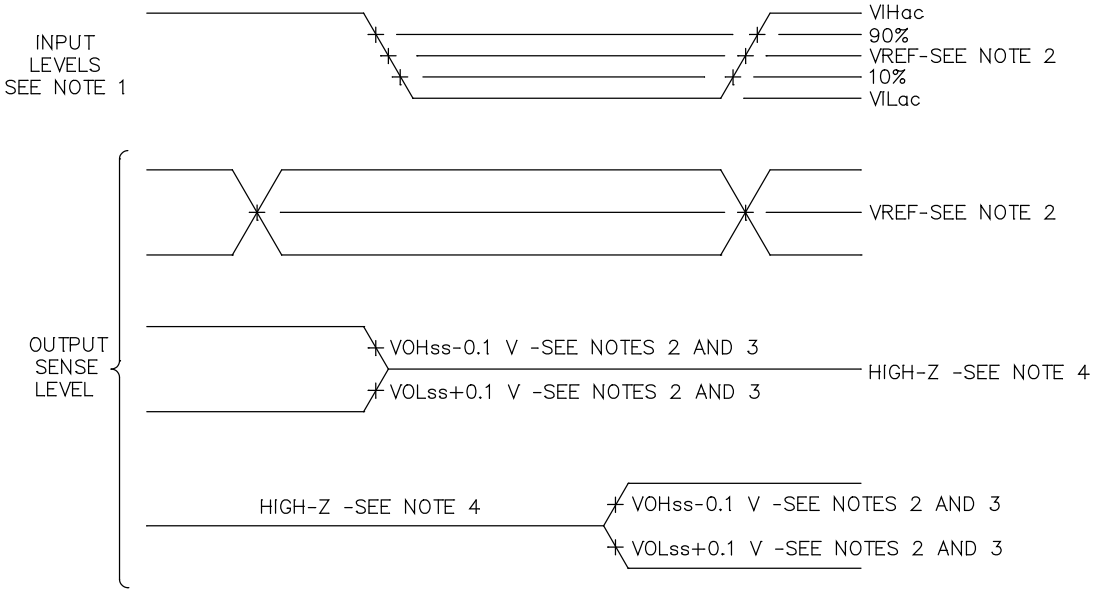
1/ V_{IN} for Don't care (X) inputs = V_{IL} or V_{IH}.
2/ When NOE = high, I/O is high Z.
3/ To dissipate the minimum amount of standby power when in standby mode: NCS = V_{CC} and CE = GND. All other input levels may float.

FIGURE 3. Truth table.

AC Timing Output Load Circuit



NOTE 1: Set to 5 pF for T*QZ (Low-Z to High-Z) timing parameters.

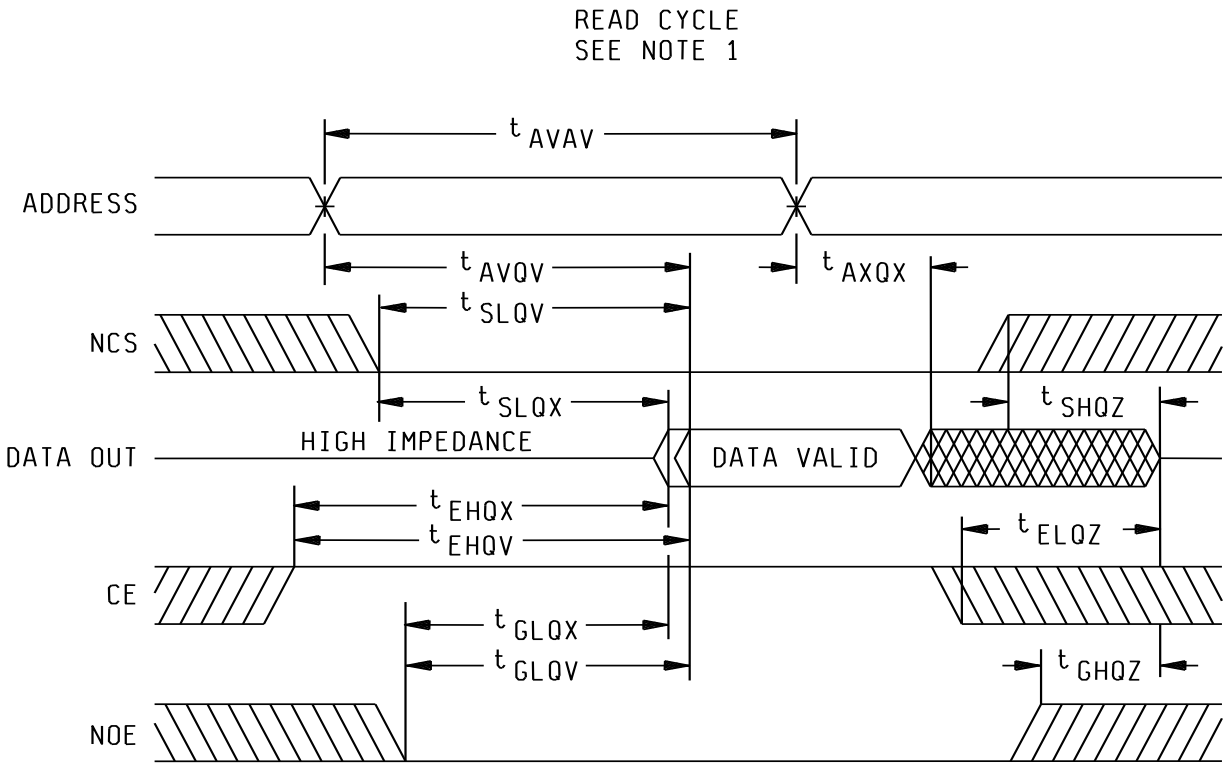


NOTES:

1. All input rise and fall times = 1 ns between the 90% and 10% levels
2. Timing parameter reference voltage level.
3. ss: Low-Z V_{OH} and V_{OL} steady state output voltage.
4. High-Z output pin pulled to V_{LOAD} by output load circuit.

I/O type	$V_{IH}ac$	$V_{IL}ac$	V_{REF}	V_{LOAD}
5.0 V CMOS	V_{DDIO} – 0.5 V	V_{SS} + 0.5 V	$V_{DDIO}/2$	$V_{DDIO}/2$
5.0 V TTL	3.0 V	0.0 V	1.5 V	1.5 V

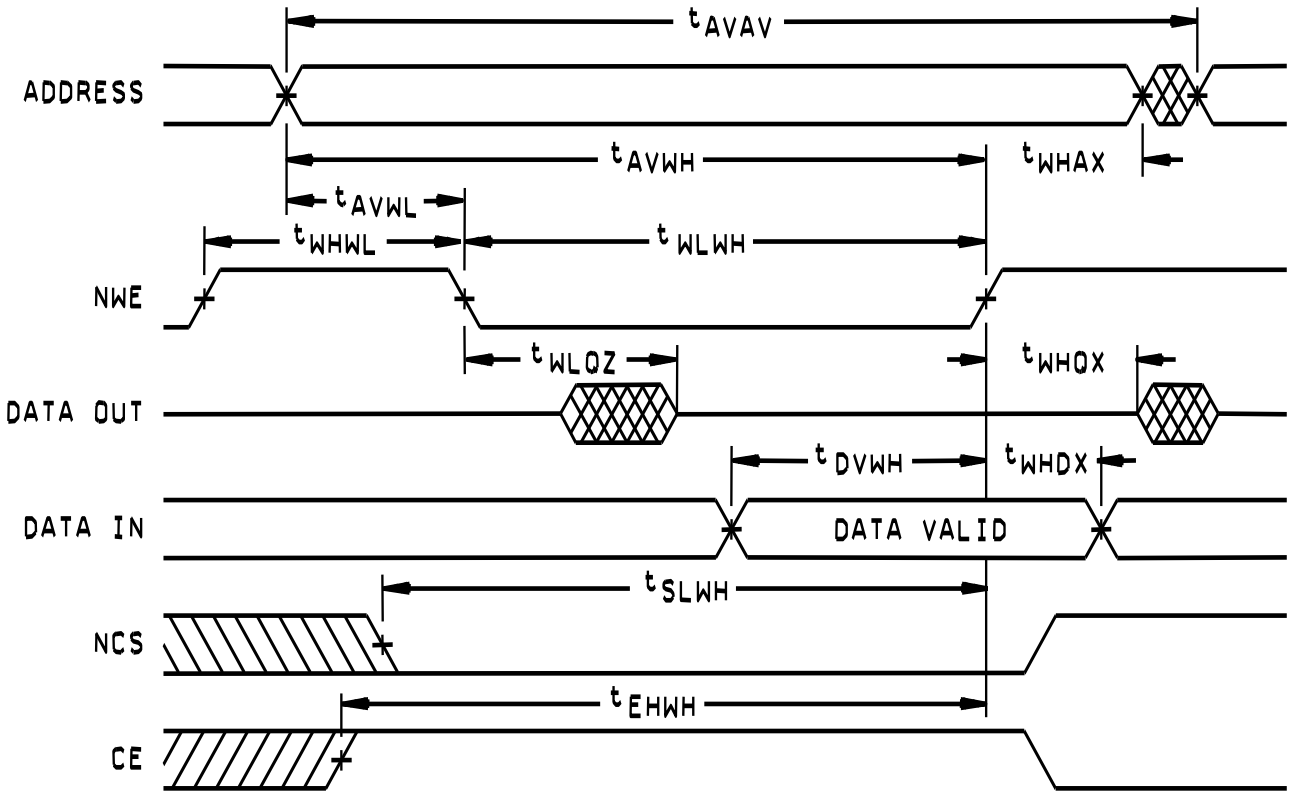
FIGURE 4. Output load circuit.



NOTE 1: NWE is high for read cycle.

FIGURE 5. Timing waveforms.

WRITE CYCLE
SEE NOTES 1,2,3,4,AND 5



NOTES:
1. Write cycle data is latched by the first occurrence of NCS high, CE low or NWE high.
2. NCS high, CE low, or NWE high must occur while address transitions.
3. Write cycle time is guaranteed for toggling NCS and CE or holding NCS or CE, or both, in active state.
4. The worst case timing sequence of t_{WLQZ} + t_{DVWH} + t_{WHWL} = the write cycle time (t_{AVAV}).
5. NOE high will eliminate the I/O output from becoming active (t_{WLQZ}).

FIGURE 5. Timing waveforms - continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required
3	Same as line 1		1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1		1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the functionality for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.
4/ * indicates PDA applies to subgroup 1, 7 and Δ.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta value shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
$I_{DDSB(standby)}$	± 10% of specified value in table IA
I_{ILK}, I_{OLK}	± 10% of specified value in table IA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta (Δ).

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

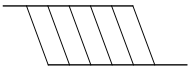
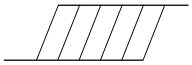
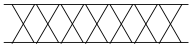
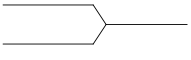
6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional date shall be supplied:

a. RHA test conditions of SEP.

b. Number of upsets (SEP).

c. Number of transients (SET).

d. Occurrence of latchup (SEL).

APPENDIX A

Appendix A forms a part of SMD 5962-98537

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

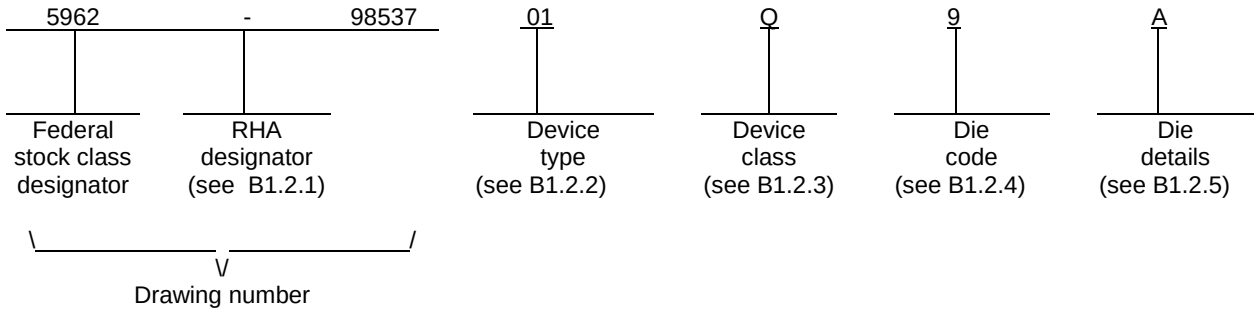
Appendix B

Appendix B forms a part of SMD 5962-98537

B.1 Scope

B.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

B.1.2 PIN. The PIN is as shown in the following example:



B.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

B.1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Input/output levels	Chip enable	Access time
01		128K X 8 Rad-Hard CMOS/SOI SRAM	CMOS	Dual	25 ns
02		128K X 8 Rad-Hard CMOS/SOI SRAM	TTL	Dual	25 ns

B.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

B.1.2.4 Die code. The die code designator shall be a number 9 for all devices supplied as die only with no case outline.

B.1.2.5 Die details. The die details designation is a unique letter, which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

B.1.2.5.1 Die physical dimensions.

Device type	Die size	Die thickness	Die Detail	Figure Number
01	443.7 mils X 446.8 mils	15± 0.5 mils	A	B-1
02	443.7 mils X 446.8 mils	15± 0.5 mils	A	B-1

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-HDBK-103.

B.1.2.5.2 Die bonding pad locations and electrical functions.

Device type	Die Detail	Figure Number
01	A	B-1
02	A	B-1

B.1.2.5.3 Interface materials.

Device type	Top metalization	Backside metalization	Die Detail	Figure Number
01	Al/Cu, 9kÅ - 11.0 kÅ	None (backgrind)	A	B-1
02	Al/Cu, 9kÅ - 11.0 kÅ	None (backgrind)	A	B-1

B.1.2.5.4 Assembly related information.

Device type	Glassivation	Die Detail	Figure Number
01	Nitride 9kÅ	A	B-1
02	Nitride 9kÅ	A	B-1

B.1.2.5.5 Wafer fabrication source.

Device type	Source	Die Detail	Figure Number
01	Honeywell SSEC, Plymouth	A	B-1
02	Honeywell SSEC, Plymouth	A	B-1

B.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

B.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

B.2 APPLICABLE DOCUMENTS.

B.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

B.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

B.3 REQUIREMENTS.

B.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-389535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The Modification in the QM plan shall not effect the form, fit or function as described herein.

B.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

B.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in B.1.2.5.1 and on figure B-1.

B.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in B.1.2.5.2 and on figure B-1.

B.3.2.3 Interface materials. The interface materials for the die shall be as specified in B.1.2.5.3 and on figure B-1.

B.3.2.4 Assembly related information. The assembly related information shall be as specified in B.1.2.5.4 and figure B-1.

B.3.2.5 Truth table(s). The truth table(s) shall be as defined in paragraph 3.2.3 herein.

B.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

B.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

B.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in B.1.2 herein. The certification mark shall be "QML" or "Q" as required by MIL-PRF-38535.

B.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see B.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

B.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

B.4 VERIFICATION

B.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

B.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a. Wafer lot acceptance for Class V product using the criteria within MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph B.3.4).

c. 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883, method 2010 or the alternate procedures allowed within MIL-STD-883, method 5004.

B.4.3 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed including groups A, B, C, D and E inspections and as specified herein except where MIL-PRF-38535 permits alternate in-line control testing.

B.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see B.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535.

B.5 DIE CARRIER

B.5.1 Die carrier requirements. The requirements for the die carrier shall be in accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

B.6 NOTES

B.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit application (original equipment), design applications, and logistics purposes.

B.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, Columbus, Ohio, 43218-3990 or telephone (614) 692-0540.

B.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-HDBK-1331.

B.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see B.3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

1 MEG - 22018541
HX6228

CHIP SIZE (after saw)	11,270µm 443.7 mil	11,349µm 446.8 mil
CHIP SIZE*	11,320µm 445.7 mil	11,4009µm 448.8 mil
Lower Left*	-5737.5	-5990.0
Upper Right*	5582.5	5410.0

* Saw Center to Saw Center

Pad List	X (µm)	Y(µm)	Signal
01	-5542.50	5180.50	VSS*
02	-5542.50	4985.50	BSC
03	-5542.50	4790.50	VDD*
04	-5542.50	4515.15	A11
05	-5542.50	3762.55	A9
06	-5542.50	3463.65	A8
07	-5542.50	2711.05	A13
08	-5542.50	2447.50	VSS*
09	-5542.50	2145.20	VDD*
10	-5542.50	1875.75	NWE
11	-5542.50	1315.95	CE
12	-5542.50	1017.05	A15
13	-5542.50	264.45	A16
14	-5542.50	-1174.25	A14
15	-5542.50	-1473.15	A12
16	-5542.50	-2225.75	A7
17	-5542.50	-2570.20	VDD*
18	-5542.50	-2872.50	VSS*
19	-5542.50	-3216.95	A6
20	-5542.50	-3969.55	A5
21	-5542.50	-4268.45	A4
22	-5542.50	-5021.05	A3
23	-5542.50	-5290.50	VDD*
24	-5542.50	-5559.95	BSC
25	-5542.50	-5755.50	VSS*
26	5405.50	-5751.90	VSS*
27	5405.50	-5556.90	BSC
28	5405.50	-5361.90	VDD*
29	5405.50	-5092.45	A2

FIGURE B-1. Bond Pad Locations and Functions for Device 01 and 02.

Pad List	X (µm)	Y(µm)	Signal
30	5405.50	-4338.25	A1
31	5405.50	-4039.35	A0
32	5405.50	-3512.80	VSS
33	5405.50	-3204.60	TTL
34	5405.50	-2905.70	VDD
35	5405.50	-2452.60	D0
36	5405.50	-2153.70	D1
37	5405.50	-1398.60	D2
38	5405.50	-1099.70	D3
39	5405.50	57.15	VSS*
40	5405.50	297.15	VDD*
41	5405.50	794.70	D4
42	5405.50	1093.60	D5
43	5405.50	1848.70	D6
44	5405.50	2147.60	VDD
45	5405.50	2343.00	VSS
46	5405.50	2641.90	D7
47	5405.50	3396.55	NCS
48	5405.50	3695.45	A10
49	5405.50	4449.65	NOE
50	5405.50	4719.10	VDD*
51	5405.50	4988.55	BSC
52	5405.50	5184.10	VSS*

FIGURE B-1. Bond Pad Locations and Functions for Device 01 and 02 - Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-05-28

Approved sources of supply for SMD 5962-98537 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9853701QXC	34168	HX6228/TQHC
5962H9853701VXC	34168	HX6228/TVHC
5962H9853701QYC	34168	HX6228/AQHC
5962H9853701VYC	34168	HX6228/AVHC
5962H9853702QXC	34168	HX6228/TQHT
5962H9853702VXC	34168	HX6228/TVHT
5962H9853702QYC	34168	HX6228/AQHT
5962H9853702VYC	34168	HX6228/AVHT
5962H9853701Q9A	34168	HX6228Die
5962H9853702Q9A	34168	HX6228Die

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34168	Honeywell Aerospace 12001 State Highway 55 Plymouth, MN 55441

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.